Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 1 to show the legend "Prior Art." This sheet replaces the original sheet showing Fig. 1.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Claims 1-10, 12-22, and 24-31 are pending in the subject application. Claims 1-24 have been examined and stand rejected. By the above amendments, claims 11 and 23 have been canceled, claims 1, 3, 7, 9, 10, 13, 15, 19, 21, 22, and 24 have been amended, and new claims 25-31 have been added. Favorable reconsideration of the application and allowance of all of the pending claims are respectfully requested in view of the above amendments and the following remarks.

With regard to formal matters, Applicant includes herewith a replacement sheet and an annotated sheet showing changes, in which the legend "Prior Art" has been added to Fig. 1. Further, the dependency of claim 24 has been changed to address the objection noted by the Examiner.

Claims 1-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,097,621 (Mori) and U.S. Patent Application Publication No. 2002/0130384 (Aton). Applicant respectfully traverse this rejection for the following reasons.

Claims 1 and 15 set forth a semiconductor memory comprising a plurality of memory cells forming at least one memory cell array. The memory cells are connected to first lines and second lines at crossing points, wherein the first lines run divergently with respect to one another, and the second lines are curved. Thus, these claims require both a set of divergent lines and a set of curved lines. No combination of the teachings of Mori and Aton suggests the combination of first divergent lines and second curves lines.

In Mori, the Examiner focuses on word lines 310a-c shown in Fig. 3, equating these word lines with the claimed first divergent lines. Each of Mori's word lines 310a-c has a "zigzag shape" and follows a serpentine path. However, these serpentine paths of Mori's word lines do not "run divergently" as required by claims 1 and 15. Rather, as shown in Mori's Fig. 3, the word lines meander along directions that are parallel relative to each other. Presumably, the Examiner is arguing that certain segments of Mori's word lines diverge, thereby meeting the claim requirement. However, other segments of Mori's word lines converge and still other segments are parallel, with a net effect that Mori's word lines run parallel to each other, not

divergently. Note, for example, that Mori's word lines 310a and 310c are always parallel and never divergent at any point. Further, when word line 310b temporarily diverges with word line 310a, it is converging with word line 310c. At no point are any of Mori's word lines diverging from each of its adjacent word lines. In short, Mori's parallel-running serpentine word lines do not run divergently with respect to each other, as required by claims 1 and 15.

Moreover, as the Examiner acknowledges, Mori fails to disclose the second, curved lines required by claims 1 and 15. As shown in Fig. 3, Mori's word and bit lines are arranged in a rectangular grid, with the word lines running in one direction (parallel to each other) and the bit lines running in a direction perpendicular to the word lines. Mori's bit lines 314a-e are perfectly straight. The Examiner relies on Aton for a teaching of curved or angles bit or word lines, arguing that it would have been obvious to use curved bit lines in Mori's device as a matter of design choice. Applicant respectfully disagrees.

As a preliminary matter, Aton's disclosure includes only a single, passing mention in paragraph [0028] that it is possible to configure word or bit lines to be curved. There is no embodiment described or shown in Aton illustrating how curved word or bit lines might be arranged or how to configured a memory array to incorporate curved word or bit lines. More particularly, there is no suggestion or teaching in Aton to include the combination of divergent lines and curved lines in a memory array.

Even assuming Aton generally suggests the possibility of curved word or bit lines, it would not have been obvious to incorporate curved bit lines in Mori's memory cell array as suggested by the Examiner. As previously noted, Mori's memory cell array is a rectangular grid with straight bit lines. Mori's rectangular grid could not be realized with curved bit lines. In contrast, curved lines are suitable in the context of the present invention, because they complement the other lines which run divergently (see, e.g., Figs. 2-5). In any event, there is no motivation or suggestion in Mori's or Aton's disclosures to fundamentally modify the layout of Mori's memory array to accommodate curved bit lines. More generally, no combination of Mori and Aton fairly suggests employing a combination of divergent and curved bit/word lines in a

memory array. Consequently, the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 1 and 15 and their dependent claims.

With regard to certain dependent claims, claims 2 (2/1) and 14 (14/13) require the first lines to extend divergently from a logic area to the memory cells, claims 3 (3/1) and 15 (15/13) require the memory cells to have the form of an annular portion with first lines diverging radially and the second lines curving arcuately, and claims 4 (4/1) and 16 (16/13) require the memory cell arrays to surround a logic area annularly. None of these claim requirements is suggested by either of the cited references. The Examiner argues that Mori's word lines "run divergently from a logic area (not shown) in a radial fashion." Applicant respectfully disagrees. Not only is the alleged logic area not shown by Mori, it is not disclosed in any manner. Moreover, there are certainly no radially diverging or arcuately curving word or bit lines or annular memory cell arrays disclosed anywhere in Mori or Aton. Thus, for these additional reasons, these dependent claims should be allowable over the cited references.

Applicant has added new claims 25-31 as follows. Claims 25 (25/1) and 28 (28/13) require the first lines to run divergently in non-parallel directions along their extent. Claims 26 (26/1) and 29 (29/13) require the first lines to be continuously divergent along their extent. Claims 27 (27/1) and 30 (30/13) require the second lines to extend along concentric arcs. Finally, new independent claim 31 sets forth a semiconductor memory comprising: a centrally-located logic area for operating the semiconductor memory; at least one memory array surrounding the logic area; first lines extending outward from the logic area into the at least one memory array; second lines extending through the at least one memory array along a periphery of the logic area and arranged concentrically with respect to the logic area such that the first and second lines form a non-rectangular array of crossing points; and a plurality of memory cells coupled to the first and second lines at the crossing points, the memory cells including storage capacitors laterally offset alternately on each side of respective first lines or respective second lines. Support for these claims is shown in Figs. 2-5. None of these claim requirements is suggested by the cited references; accordingly, the Examiner is respectfully requested to find these claims in condition for allowance.

In view of the foregoing, Applicant respectfully requests the Examiner to find the application to be in condition for allowance with claims 1-10, 12-22, and 24-31. However, if for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

Filed concurrently herewith is an excess claim fee in the amount of $250 for five claims in excess of the twenty-four previously paid for. Applicant hereby petitions for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Respectfully submitted,

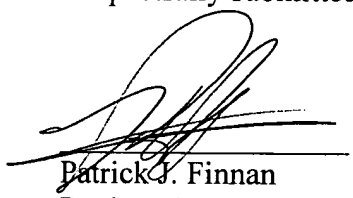

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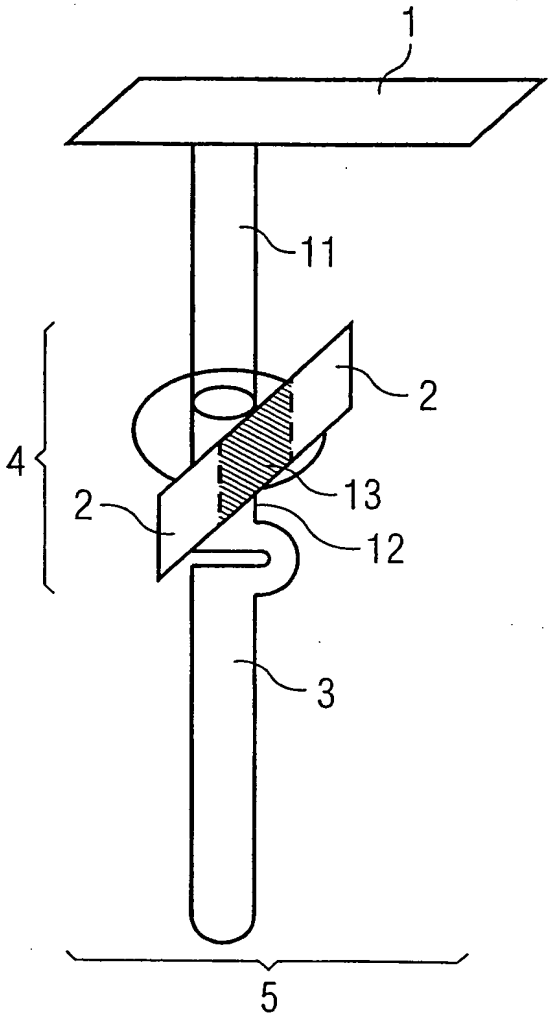
FIG 1



PRIOR ART